



CanSat Leader Training Program (CLTP) 5

Applicant Background Assessment Test

November 2013

Deadline for submission: Friday, February 28, 2014 (17:00, Japan Standard Time)







APPLICANT BACKGROUND ASSESSMENT TEST FOR CANSAT LEADER TRAINING PROGRAM (CLTP) 5

INTRODUCTION

The main objective of the CanSat Leader Training Program (CLTP) is to build space technology skills and to improve teaching methods in space engineering education. To achieve these objectives, the number of facilitators who can lead CanSat projects in different regions around the world needs to be increased. This program is designed to provide future CanSat project leaders with a quality space engineering education course based on the Japanese CanSat program. To participate in a laboratory workshop, program applicants should have basic knowledge of aerodynamics, programming, linear algebra, electronic circuits, and mechanical production. The following test is designed to assess the applicant's knowledge in the aforementioned engineering disciplines. This test is part of the application for CLTP5, so a copy must be submitted in pdf format along with the online application form at https://www.cltp-online.info/application_form.php, or emailed directly to the CLTP office at work.

GENERAL INSTRUCTIONS

- 1. Answer all questions in the space provided below each question. If the space is not sufficient, please continue your answer on a separate sheet of paper and attach it to the application in sequence. Do not write any answers on the back side of a page.
- 2. Make reasonable assumptions if any data is missing, and remember that neatness is important.
- 3. The applicant may use ONLY published material to help in answering a question.
- 4. Answers should be supported with a sketch if applicable.
- 5. The test answers must be submitted in pdf format along with the online application form at https://www.cltp-online.info/application_form.php, or emailed directly to the CLTP office at secretariat@cltp.info by the deadline given above.

APPLICANT INFORMATION

1 Full name in Roman

characters

(use block capital letters)

| | | Family name | First name | Middle name | \Box Male |
|---|------------------------|--------------------------|--------------|-------------|---------------|
| | (*)Write your name exa | ctly as it appears in yo | our passport | | \Box Female |
| 2 | Nationality | | | | |
| 3 | Affiliation | | | | |





[Q-1] (Analog circuits)

Consider two types of LEDs, D1 and D2, with the properties shown below. Answer the following questions.

(1) What term is used to refer to a resistance such as R1?

(2) In circuit A, what is the value of resistance R1 necessary to make LED D1 turn on?

(3) In circuit B, what values for resistances R1 and R2 are necessary to make LEDs D1 and D2 turn on?

| | Maximum | | | | | |
|----|-----------------|---------------------------------|---------|---------------------|--------------------|--|
| | Forward Current | Forward Voltage Forward Current | | Dominant Wavelength | Luminous Intensity | |
| | (mA) | VF (V) | IF (mA) | λD (nm) | Iv (mcd) | |
| D1 | 20 | 2.0 | 10 | 630 | 10 | |
| D2 | 25 | 2.1 | 15 | 572 | 16 | |



Circuit A

Circuit B





[Q-2**]** (Truth tables for digital circuits)

The digital circuit drawn below has two inputs, S and R, and two outputs, Q and ~Q.

(1) Construct the truth table for the inputs and outputs as shown in the circuit.

(2) This circuit has some essential properties and finds application in some important devices. Describe the properties and give some examples of applications.







[Q-3] (Algorithms)

A certain CPU has six 8-bit registers—named A, B, C, D, E, and F—for operations. The registers can be used in pairs as AF, BC, and DE to allow for three 16-bit registers, but no other pairings are allowed.

The following is a list of available operations.

| Operation Code | Operand(s) | Implementation, where X and Y are registers and <i>n</i> is a number. | |
|----------------|-------------|--|--|
| | | NOTE: The number of bits must coincide, for example, | |
| | | 'ADD A, B' is allowed but 'ADD A, BC' is not. | |
| ADD | Χ, Υ | X = X + Y or X += Y | |
| ADD | X, <i>n</i> | X = X + n or X + = n | |
| SUB | Χ, Υ | X = X - Y or $X = Y$ | |
| SUB | X, <i>n</i> | X = X - n or X - = n | |
| INC | Х | ++X (in C language) | |
| DEC | Х | X (in C language) | |
| LD | Х, Ү | X = Y | |
| LD | X, <i>n</i> | X = n | |
| SRL | Х | Logical right-shift. 'SR X' as $X=10110101$ yields the new X as $X=01011010$. | |
| SLL | Х | Logical left-shift. 'LR X' as X=10110101 yields the new X as X=01101010. | |
| JP | LOOP | Unconditional jump to the line labeled LOOP. | |
| JPZ | X, LOOP | Conditional jump. If X=0, then jump to the line labeled LOOP. | |
| JPNZ | X, LOOP | Conditional jump. If not $(X = 0)$, then jump to the line labeled LOOP. | |
| PUSH | X | Copy the value of X to the specified memory location. | |
| POP | X | Copy the value in the specified memory location to X. | |
| END | | CPU halts the process. | |

For example, the following operations swap the values of registers A and B.

LD C, A LD A, B LD B, C

A loop with 10 iterations can be implemented as follows.

LD A, 10 LOOP: Procedure 1 Procedure 2

> DEC A JPNZ A, LOOP

With this in mind, write a program that takes the values stored in registers C, D, E, and F and stores them in order of descending value in registers C, D, E, and F, in this order.









[Q-4**]** (Element selection and datasheet preparation)

An element satisfying the following requirements is wanted.

Using a suitable method, find an element that satisfies all the listed requirements and indicate its model number and manufacturer.

Also, prepare a datasheet about that element and attach it to the answer as a PDF file or as a scanned image.

Remarks)

Elements of the same model can have different model numbers; these correspond to slightly different specifications and packaging.

For example, for the AD623 instrumentation amplifier by Analog Devices, there are two models, AD623A and AD623B; these have different maximum input offset voltages and different maximum input offset drifts.

Another example is the TL431 precision programmable reference by Texas Instruments, which is found as the TL431CPL model (with TO-92 package and guaranteed operation between 0 and 70 °C), the TL431IP model (with SOIC package and guaranteed operation between -40 and 85 °C) and so on.

Requirements

- Source voltage of 5 V.
- Operating temperature range -50 to 80 °C.
- DIP (Dual Inline Package)
- Output current of 100 mA.
- Uses an external trigger to produce a pulse output in one-shot timer mode.
- The duration of the output pulse can be set to an arbitrary value by an external element.





I hereby certify that I have completed the background assessment test for CLTP5 without any help or assistance from others.

Date:

Applicant's signature:

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Applicant's name in Roman characters (use block capital letters):